120 is formed. In the process 510, the conductive region may correspond to the source/drain region 120.

[0260] In a process 520, a contact hole, which penetrates the dielectric and exposes the conductive region, may be formed.

[0261] In some example embodiments, to perform the process 520, using the method as described with reference to FIGS. 9A to 9B, the contact hole CH penetrating the interlayer dielectric 136 and the inter-gate dielectric 132 may be formed by sequentially etching the interlayer dielectric 136 and the inter-gate dielectric 132.

[0262] In a process 530, the substrate, in which the contact hole is formed, may be cleaned.

[0263] In some example embodiments, to perform the process 530, using the method as described with reference to FIGS. 9A to 9B, the substrate 110, in which the contact hole CH is formed, may be cleaned.

[0264] In a process 540, a metal film contacting the conductive region may be formed in the contact hole.

[0265] In some example embodiments, to perform the process 540, using the method as described with reference to FIGS. 10A to 10B, the metal film 130 contacting the source/drain region 120 may be formed in the contact hole CH.

[0266] In a process 550, a conductive barrier film covering an inner wall of the contact hole may be formed on the metal film.

[0267] In some example embodiments, to perform the process 550, using the method as described with reference to FIGS. 11A to 11B, the conductive barrier film 150 covering the metal film 130 inside and outside the contact hole CH may be formed.

[0268] In some example embodiments, the process 540 and the process 550 may be consecutively performed in situ in the integrated circuit device fabricating apparatus 400 shown in FIG. 22 without vacuum break.

[0269] In a process 560, a metal silicide film may be formed by performing silicidation of at least a portion of the metal film using a silicidation atmosphere while the conductive barrier film is exposed to the silicidation atmosphere.

[0270] In some example embodiments, to perform the process 560, using the method as described with reference to FIGS. 12A to 12B, the metal silicide film 140 may be formed by performing silicidation of at least a portion of the metal film 130 using a silicidation atmosphere while the conductive barrier film 150 is exposed to the silicidation atmosphere.

[0271] In some example embodiments, the process 550 and the process 560 may be consecutively performed in situ in the integrated circuit device fabricating apparatus 400 shown in FIG. 22 without vacuum break. In some example embodiments, the process 550 and the process 560 may be performed in the same chamber.

[0272] In a process 570, a composition-changed conductive barrier film may be formed by treating the conductive barrier film covering the metal silicide film in an atmosphere including at least one of nitrogen and hydrogen in an apparatus which includes a cluster tool including a plurality of process chambers.

[0273] In some example embodiments, the cluster tool may be configured as the integrated circuit device fabricating apparatus 400 described with reference to in FIGS. 22 to 24.

[0274] In some example embodiments, to perform the process 570, using the method as described with reference to FIGS. 13A to 13B, the composition-changed conductive barrier film 150A may be formed by treating the conductive barrier film 150 (see FIGS. 12A and 12B) covering the metal silicide film 140 in the atmosphere 152 including at least one of a nitrogen atom and a hydrogen atom.

[0275] In some example embodiments, to perform the process 570, at least one process chamber 420 selected from among the plurality of process chambers 420 included in the integrated circuit device fabricating apparatus 400 shown in FIG. 22 may be used. The chamber performing the process 570 among the plurality of process chambers 420 may be a plasma treatment chamber, a heat treatment chamber, or a UV treatment chamber. For example, the chamber performing the process 570 may be the process chamber 420A shown in FIG. 23, or the process chamber 420B shown in FIG. 24.

[0276] In some example embodiments, the process 560 and the process 570 may be consecutively performed in situ in the integrated circuit device fabricating apparatus 400 shown in FIG. 22 without vacuum break.

[0277] In a process 580, using the apparatus including the cluster tool, a metal plug filling the contact hole may be formed on the composition-changed conductive barrier film.

[0278] In some example embodiments, to perform the process 580, using the methods as described with reference to FIGS. 14A to 17B, the metal plug 160P filling the contact hole CH may be formed on the composition-changed conductive barrier film 150A.

[0279] In some example embodiments, to perform the process 580, at least two process chambers 420 selected from among the plurality of process chambers 420 included in the integrated circuit device fabricating apparatus 400 shown in FIG. 22 may be used. For example, the process of forming the metal seed layer 162, which is described with reference to FIGS. 14A and 14B, may be performed using a PVD, CVD, or ALD chamber included in the plurality of process chambers 420, the process of forming the metal filling layer 164, which is described with reference to FIGS. 15A and 15B, may be performed using a CVD chamber included in the plurality of process chambers 420, and the reflow process of the metal seed layer 162 and the metal filling layer 164, which is described with reference to FIGS. 16A and 16B may be performed in the same chamber as the chamber used for forming the metal filling layer 164. The reflow process may be performed by heating the substrate 110 to a temperature of about 200° C. to about 500° C. The process of forming the metal seed layer 162, the process of forming the metal filling layer 164, and the reflow process may be consecutively performed using the integrated circuit device fabricating apparatus 400 shown in FIG. 22, without vacuum break.

[0280] In some example embodiments, the process 570 and the process 580 may be consecutively performed in situ in the integrated circuit device fabricating apparatus 400 shown in FIG. 22, without vacuum break.

[0281] FIG. 26 is a graph depicting a change in resistance Rs of a conductive barrier film formed in accordance with a method of fabricating an integrated circuit device in accordance with an example embodiment of the inventive concepts, and a change in oxygen content in the conductive barrier film, as measured along with process stages for forming the conductive barrier film.